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Via patterning in the 7-nm node using immersion lithography and graphoepitaxy directed self-assembly

Jan Doise,[a,b,*] Joost Bekaert,[b] Boon Teik Chan,[b] Masafumi Hori,[c] and Roel Gronheid[b,†]
[a]KU Leuven, Department of Electrical Engineering (ESAT), Heverlee, Belgium
[b]IMEC, Heverlee, Belgium
[c]JSR Micro N.V., Leuven, Belgium

Abstract. Insertion of a graphoepitaxy directed self-assembly process as a via patterning technology into integrated circuit fabrication is seriously considered for the 7-nm node and beyond. At these dimensions, a graphoepitaxy process using a cylindrical block copolymer that enables hole multiplication can alleviate costs by extending 193-nm immersion-based lithography and significantly reducing the number of masks that would be required per layer. To be considered for implementation, it needs to be proved that this approach can achieve the required pattern quality in terms of defects and variability using a representative, aperiodic design. The patterning of a via layer from an actual 7-nm node logic layout is demonstrated using immersion lithography and graphoepitaxy directed self-assembly in a fab-like environment. The performance of the process is characterized in detail on a full 300-mm wafer scale. The local variability in an edge placement error of the obtained patterns (4.0 nm 3σ for singlets) is in line with the recent results in the field and significantly less than of the prepattern (4.9 nm 3σ for singlets). In addition, it is expected that pattern quality can be further improved through an improved mask design and optical proximity correction. No major complications for insertion of the graphoepitaxy directed self-assembly into device manufacturing were observed. [DOI: 10.1117/1.JMM.16.2.023506]

Keywords: block copolymer; directed self-assembly; via patterning; graphoepitaxy; logic layout.

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1 Introduction

Directed self-assembly (DSA) of block copolymers (BCP) has attracted significant research attention as a patterning approach for future generation integrated circuits.[1–4] One of the areas where DSA is considered to have a high potential to be integrated into device manufacturing in the near future is the patterning of holes using a graphoepitaxy process with a cylindrical phase BCP.[5,6] In graphoepitaxy, lithography is used to create a topographical prepattern in which a BCP is deposited and allowed to phase separate. In case a cylindrical phase BCP is applied, this gives a straightforward approach to pattern randomly distributed contact holes such as found in logic via layers. Application of DSA in this way allows for an extension of 193-nm immersion lithography while reducing the number of needed masks compared with the conventional multiple patterning techniques.[5,7] As a result, the implementation of graphoepitaxy DSA as patterning technology is an opportunity to avoid the use of high cost approaches such as extreme ultraviolet lithography and traditional multiple patterning methods.

For insertion of graphoepitaxy DSA into device manufacturing to be successful, a number of challenges still need to be addressed. Among these are defects, pattern variability in terms of hole size and placement, and DSA-aware design. Although considerable progress has been made in the field,[8–11] these results are commonly generated with periodic layouts. It is important to verify these results using a representative layout for the intended application for two main reasons. First, the graphoepitaxy processes are known to be impacted by fluctuations in template pattern density[12–14] found in aperiodic designs that are typical for logic via layouts. Second, this allows for the experimental verification of DSA-aware designs. Initial work with aperiodic designs has been done by Yi et al.[15,16] We have shown in earlier work[7] how via layouts can be decomposed for DSA using a set of relatively simple design rules. In this assessment, we found that a DSA-friendly design can reduce the number of via masks (splits) for a place-and-routed 7-nm node logic layout from four—for traditional [litho-etch]×4—to two—for [litho-etch-DSA-etch]×2. In the resulting via clip, shown in Fig. 1(a), the tightest pitches are 56 nm in the horizontal direction and 48 nm in the vertical direction (corresponding to one and two times the pitch of the metal layer to which the vias are connecting, respectively). The use of feature multiplication in the form of doublets (two-hole features) to pattern the tightest pitch of 48 nm in the vertical direction allows for the significant reduction in the number of masks and thus cost. In this work, the performance of our graphoepitaxy process flow in patterning this via clip is studied in a fab-like environment. It should be noted that, even though the relationship between BCP formulation and the resulting defectivity[17,18] is an important topic in the field, it is beyond the scope of this work.

2 Experimental

2.1 *Materials*

Spin-on-carbon (SOC) HM710 and spin-on-glass (SOG) ISX304 were acquired from JSR Micro. ArF immersion negative tone development photoresist AN02 was purchased

*Address all correspondence to: Jan Doise, E-mail: jan.doise@imec.be

†Current address: KLA Tencor/ICOS Belgium, Leuven, Belgium

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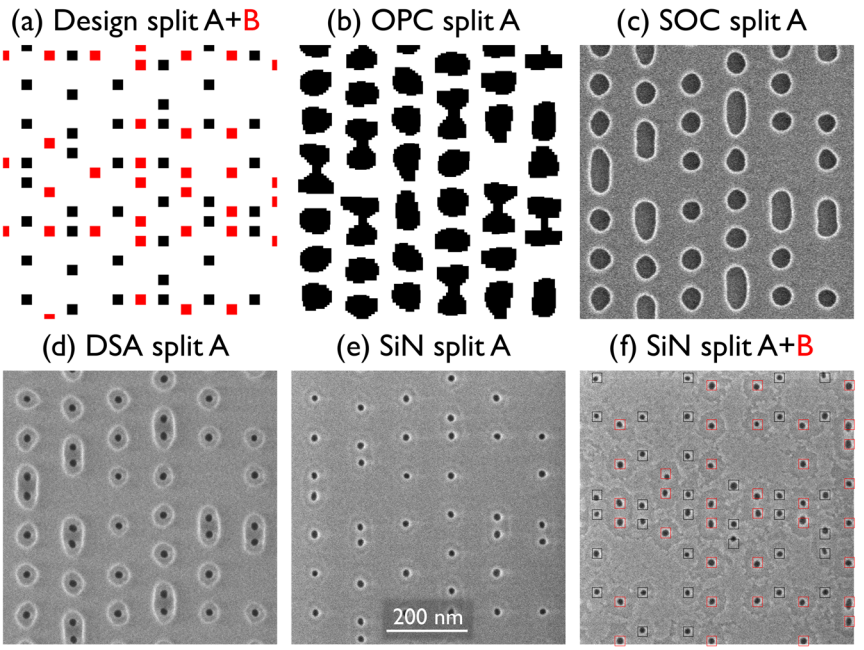

Fig. 1 Images of the logic via clip at different stages in the process. (a) Design of split A and B. (b) OPC of the templates of split A. (c) SEM image of the templates in SOC (after SOG strip) of split A. (d) SEM image of split A after PMMA removal. (e) SEM image of split A after pattern transfer into SiN. (f) SEM image of split A + B after double patterning into SiN.

from Fujifilm. End-functionalized polystyrene (PS) brushes were synthesized by JSR Micro and used as received. Organic solvent RER600 was purchased from Fujifilm. Cylindrical phase poly(styrene-*block*-methyl methacrylate) (PS-*b*-PMMA) with $M_n = 66.5$ kg mol^{-1} for PS and 28.5 kg mol^{-1} for PMMA was synthesized and blended with PS homopolymer ($M_n = 10$ kg mol^{-1}) at a weight ratio of 9:1 by JSR Micro and used as received.

2.2 *Graphoepitaxy Process Flow*

In Fig. 2, a schematic overview of the process flow is depicted. Fifty-nanometer of silicon nitride (SiN) was deposited on 300-mm silicon wafers. SOC was coated on a Tokyo Electron Clean Track Lithius Pro Z™. SOG and photoresist were coated on a Sokudo DUO coat and development system. For coating and development of the SOC, SOG, and photoresist, vendor recommended settings were used for postapply bake, postexposure bake, and development. Photoresist was patterned using an ASML NXT:1950i scanner connected to a Sokudo DUO coat and development system. Exposures were done at 1.35 NA using custom illumination with XY-polarization. The templates defined in resist were transferred into the underlying SOG and SOC by a dry etch process performed on a Tokyo Electron Tactras™ platform. Remaining SOG was removed using 0.5% hydrogen fluoride on a Tokyo Electron Cellesta™ wafer clean system. All brush and BCP processing was done on a Tokyo Electron Clean Track Act 12™. Two end-functionalized PS brushes were applied consecutively (as a dual-brush[19] approach) by spin-coating from solution, thermal annealing under a nitrogen atmosphere, and removing ungrafted polymer molecules with an organic solvent (RER600) rinse. Subsequently, the BCP-homopolymer blend was spin-coated from solution and thermally annealed under a nitrogen atmosphere. The template fill level (local BCP film thickness) was optimized by adjusting the coating spin speed and inspecting the number and types of defects in the center of the clip after PMMA removal. The template fill is expected to be in the range of 50 to 60 nm based on atomic force microscopy measurements done previously on periodic designs (data not shown). The PMMA cores were removed by DUV exposure followed by an isopropyl alcohol rinse on a Tokyo Electron Clean Track Lithius Pro Z™. Finally, transfer of the DSA holes into the underlying SiN was performed on a Tokyo Electron Tactras™ platform.

2.3 *Metrology*

Three separate wafers were processed identically until halted for metrology at the different stages in the process (after SOG strip, after PMMA removal, and after pattern transfer into SiN). Wafers were examined using a Hitachi CG-5000 or CG-6300 top-down critical dimension (CD) scanning electron microscope (SEM). On each wafer, 405 images were collected and analyzed (9 duplicate locations per die and 45 dies per wafer). Obtained CD-SEM images (with field of view 675×675 nm) were analyzed using Robust Edge Detection software from Hitachi to determine the CD and centroid position of templates in SOC (after SOG strip) and holes in SiN as well as defects in the self-assembly (after PMMA removal) and in SiN. To determine the positional error (PE) variability, the measured centroid positions of the patterns of each image were aligned toward the design by allowing translation and rotation of the set of coordinates while minimizing the sum of the squares of the PEs. Afterward, the PE was calculated as the difference between the measured centroid coordinate after alignment and the design coordinate. For PE, the reported values are 3σ taken over all locations and dies to get a larger sample size (315 measurements) per feature. This is justified as

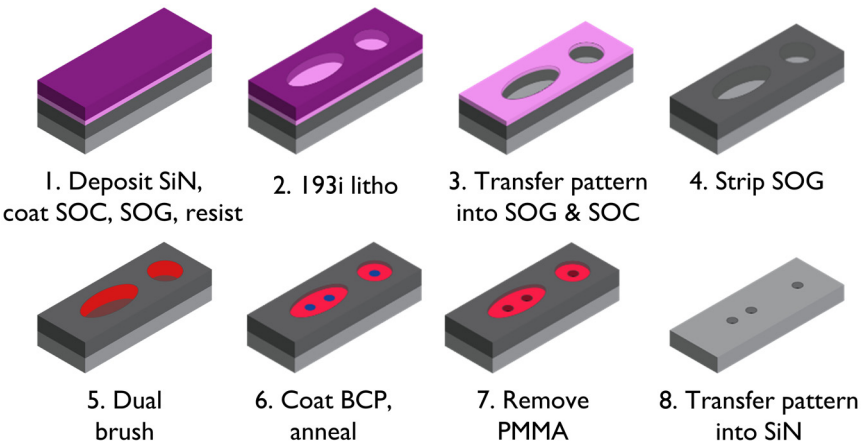

Fig. 2 Schematic overview of the graphoepitaxy process flow used.

only a limited process fingerprint across different dies was observed (see Fig. 7 in Appendix A). The design coordinates were based on the average centroid coordinates of the patterns in SOC. The design center-to-center distance for doublets was fixed for all doublet features as the average value (44 nm).

3 Results and Discussion

The process flow used in this work is schematically shown in Fig. 2 and has seen only minor changes from our earlier work.[12,20] These optimizations include a dual-brush approach for surface modification[19] and the use of a BCP–homopolymer blend[18] that increases the process window for doublets in elliptical templates. Characteristic SEM images of the via clip at different stages of the process flow are shown in Fig. 1. A detailed pattern quality assessment of split A was done on a full wafer scale (details on the sampling can be found in Sec. 2).

As shown in Table 1, the local dimensional variability of the templates in SOC is relatively high with local critical dimension uniformity (LCDU) values of 8 and 16 nm 3σ for singlets (i.e., single-hole patterns) and doublets (i.e., two-hole patterns), respectively. This is caused by large differences in average CD per individual feature [see Fig. 3(a)]. In general, more isolated templates (e.g., S1 and D1) print smaller than templates with a higher local pattern density (e.g., S3 and D3). These differences are caused by suboptimal optical proximity correction (OPC). As can be seen in Table 1, the LCDU values for individual SOC templates are much lower (e.g., 4.2 nm for S1), meaning a lower overall LCDU is possible with more extensive OPC.

Figure 4 compares the measured template dimensions on the logic clip with the process windows for singlets and doublets determined on periodic arrays. It can be seen that while the dimensions of the doublets are positioned nicely within the process window, the singlets on the clip are too small compared with the center of the process window, which leads to missing holes after self-assembly. Using a lower exposure dose during lithography to print larger singlets did not offer a good solution as it resulted in too large doublet templates that merge with adjacent templates. We determined the best exposure conditions by compromising between defects coming from respectively missing singlets and merging doublet templates.

Considering the large local variability of the templates in SOC and the offset in the average singlet template CD from the process window center, the number of defects observed after PMMA removal and after transfer into SiN (see Fig. 5) is remarkably low at 19 and 20 defects observed per 14,985 holes (measured on two separate wafers), respectively. As the majority (64%) of these defects occur on singlet templates smaller than 45 nm and doublet templates larger than 106 nm (see Fig. 8 in Appendix B), it is clear that adjusting the mask to improve the singlet template CD offset and optimizing the OPC would significantly lower the defect counts.

Figure 6 shows the average SiN CD (of all holes) and center-to-center distance (of doublets) as a function of measurement location on the clip. It can be observed that both CD and center-to-center distance show smaller values at the edges of the clip. We attribute this signature to a higher template fill level (local BCP film thickness) at these locations. A higher fill level is known to result in smaller CD after

Table 1 Summary of CD, LCDU, and PE measurements (nm) obtained in SOC.

Feature(s)	CD	LCDU	PE-X	PE-Y	EPE-X	EPE-Y
Singlets	48.1	8.2	2.1	2.6	4.6	4.9
Doublets	49.6/100.3	4.9/15.9	1.9	3.9	3.1	8.9
S1	44.3	4.2	2.0	2.3	2.9	3.1
S2	48.0	3.7	2.0	2.5	2.7	3.1
S3	51.2	4.2	2.2	3.1	3.0	3.7
D1	49.1/95.8	3.9/6.1	2.1	2.7	2.9	4.1
D2	50.1/99.1	4.0/7.3	1.9	3.2	2.8	4.9
D3	50.7/106.8	3.6/11.1	2.0	5.4	2.7	7.7

Note: LCDU values are 3σ calculated from all measurements per die, averaged over all dies. PE values are 3σ calculated from all measurements from all dies. For singlets and doublets, 3σ is calculated from measurements from all features, in contrast to data for individual features S1, S2, S3, D1, D2, and D3. For doublet CD and LCDU, numbers are given for minor axis/major axis.

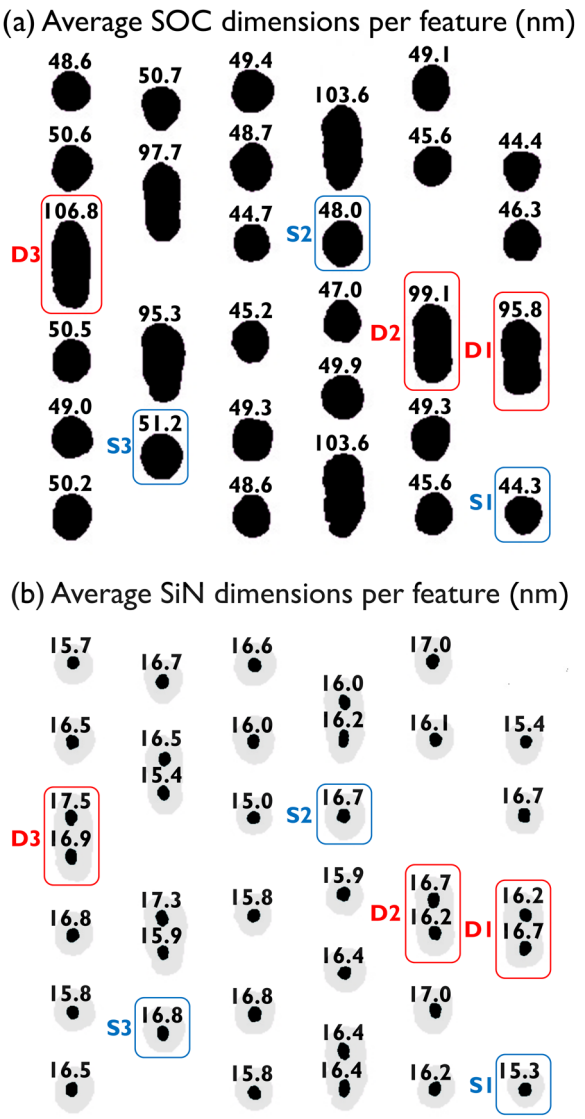

Fig. 3 Average dimensions per feature measured (a) in SOC and (b) in SiN. For doublets in SOC, the diameter along the major axis is given, and the average diameter is given for other features. Reported values are averages of all locations on all dies for (a) and averages of locations 2 → 8 on all dies for (b).

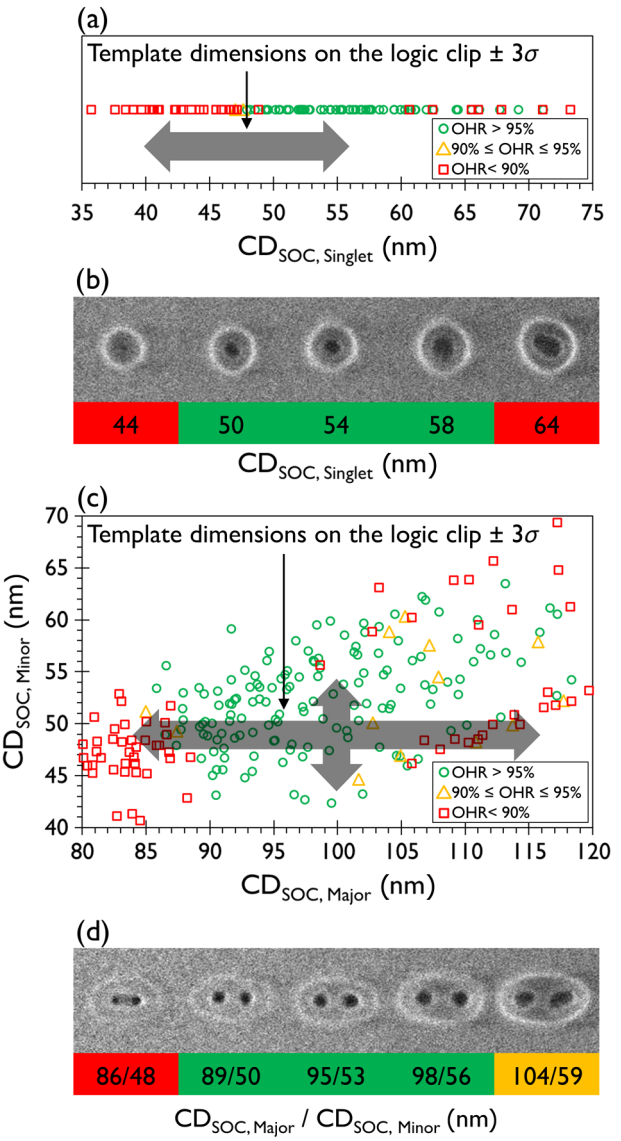

Fig. 4 Process windows of the graphoepitaxy process flow for (a) singlets in circular templates and (b) doublets in elliptical templates determined using periodic arrays. The process windows are based on open hole rate (OHR) after pattern transfer into SiN. The SOC dimensions ($\pm 3\sigma$) measured on the logic clip are indicated with an arrow overlapping the process window. Sample images across the process window are provided for (b) singlets and (d) doublets after PMMA removal.

pattern transfer[12] and we have observed that it also leads to smaller center-to-center distance of the assembled holes inside a doublet (see Fig. 9 in Appendix C). Since there is a large area adjacent to the clip with no patterns in the SOC, excess BCP material from this area will move toward the clip during the BCP anneal (as has been reported before[7]). The fact that we did not observe this signature in the SOC dimensions matches the aforementioned explanation. A 2-μm border containing dummy templates surrounding the logic structures [see Fig. 6(a)] was employed to avoid this issue but proved to be insufficient to mitigate the fill signature entirely. Because of the significant deviation of the center-to-center distance of locations 1 and 9, we did not take the CD and PE measurements (in SiN) from these locations into account. With these results in mind, we expect that increasing the dummy border width to 5 μm should be enough to circumvent the signature entirely.

As can be seen in Table 2, the measured LCDU values in SiN are substantially reduced compared with the values obtained in SOC. This can be attributed to the rectifying properties of the graphoepitaxy self-assembly process that have been consistently reported in the literature.[15,21–23] This is also nicely shown in Fig. 3, where it can be seen that the average CD difference between the smallest (S1) and the largest singlets (S3) is reduced from ~7 nm in SOC to ~1.5 nm in SiN. In addition, there is no significant difference in CD between holes originating from singlets or doublets. The LCDU of doublet holes is only slightly larger at 3.9 nm compared with 3.3 nm for singlets. Finally, no significant impact of local pattern density fluctuations is observed, in contrast to the large-scale fill signature mentioned earlier. As a result, we do not see a need to use sub-DSA-resolution assist features (i.e., an assist feature that prints but in which a nonetch-transferrable morphology

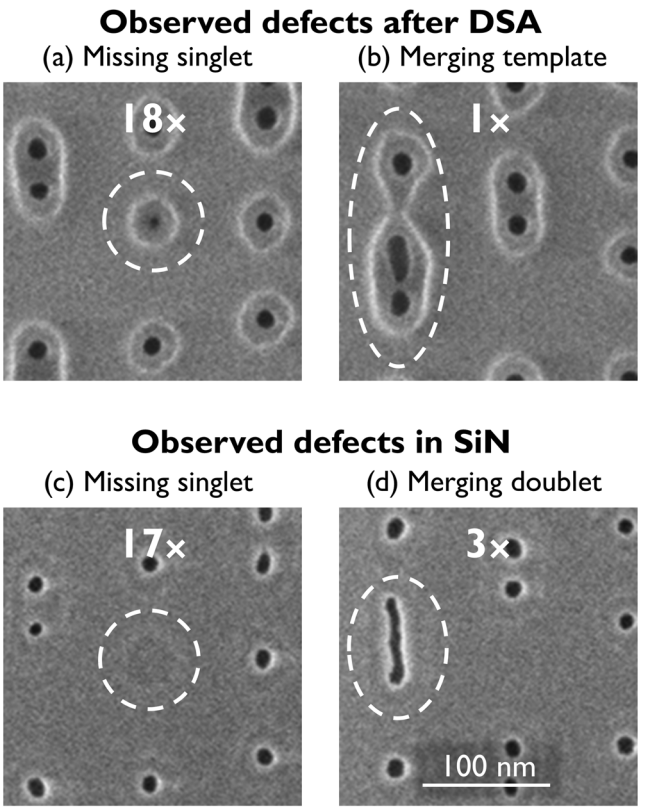

Fig. 5 Types and numbers of observed defects. After PMMA removal, (a) 18 instances of missing singlets and (b) 1 instance of merging templates were found. After SiN (on a separate wafer), (c) 17 missing singlets and (d) 3 instances of merging doublets were observed. In each case, 14,985 holes were inspected.

is formed during DSA)[7,24,25] for density effects within the patterned area in this via layout. However, they could be valuable for improving the lithographic process window[24] and consequently reducing the variability in SOC.

The variability in PE of the obtained patterns was determined by aligning the coordinate set of the measured centroids to the design (details can be found in Sec. 2). The obtained results with this method include all stochastic variations coming from the lithography, DSA, and dry etch processes. This is in contrast to the approach where both

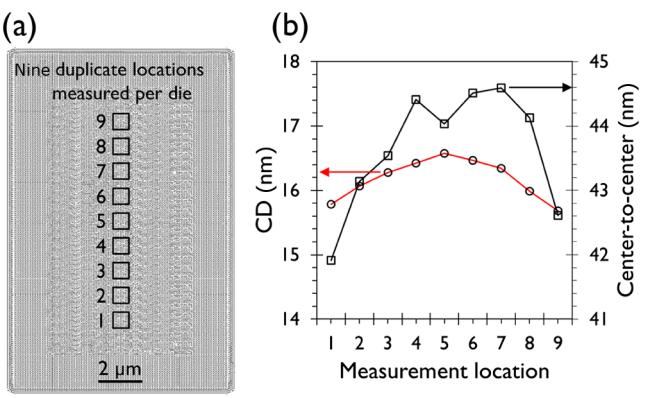

Fig. 6 Overview of (a) the measurement locations on the clip and (b) average SiN CD (of all holes) and center-to-center distance (of doublets) as a function of measurement location. Reported values are averages of all dies.

Table 2 Summary of CD, LCDU, and PE measurements (nm) obtained in SiN.

Feature(s)	CD	LCDU	PE-X	PE-Y	EPE-X	EPE-Y
Singlets	16.3	3.3	3.0	3.6	3.4	4.0
Doublets	16.5	3.9	3.2	6.0	3.7	6.3
S1	15.3	3.3	3.1	2.9	3.5	3.3
S2	16.7	2.7	2.7	3.6	3.0	3.8
S3	16.8	3.0	3.1	4.0	3.4	4.3
D1	16.5	3.1	3.4	4.7	3.7	4.9
D2	16.5	2.9	3.1	4.8	3.4	5.0
D3	17.2	4.5	3.3	8.5	4.0	8.8

Note: LCDU values are 3σ calculated from all measurements per die, averaged over all dies. PE values are 3σ calculated from all measurements from all dies. For singlets and doublets, 3σ is calculated from measurements from all features, in contrast to data for individual features S1, S2, S3, D1, D2, and D3. For doublet data, the average of the two holes is taken.

template and DSA hole centroid are determined from the same SEM image (taken after PMMA removal),[21,26] in which only the variability caused by the DSA process itself is measured. The disadvantage of the latter approach is that the image contrast after PMMA removal is quite poor due to the difference in height for the templates and the BCP film. Furthermore, the template contour is altered by the BCP coating, which adds additional variability to the metrology. Finally, doing the inspection after PMMA removal will only give information of the DSA hole placement at the top of the BCP film. The hidden three-dimensional morphology may lead to a different hole placement after pattern transfer.[27]

It can be seen in Tables 1 and 2 that for all features the PE variability is larger in the vertical than in the horizontal direction. This corresponds to the smaller pitch in the design in this direction, which results in more variability in the lithography step. For singlets, the PE variability in the vertical direction (PE-Y) increases from 2.6 nm in SOC to 3.6 nm in SiN. Doublets showed higher PE-Y with an average value of 6 nm in SiN. This higher variability can be attributed to a lower degree of confinement in addition to a larger PE and LCDU of the SOC templates in that direction. A closer look at the results for individual doublets D1, D2, and D3 provides evidence that the positional and dimensional variability of the SOC template has a significant impact. For D1 and D2, with LCDU values in SOC of 6.1 and 7.3 nm along the vertical axis, a PE-Y of 4.7 and 4.8 nm, respectively, was measured. On the other hand, for D3, with comparatively high LCDU of 11.1 nm, the PE-Y increased to 8.5 nm. Since the center-to-center distance of assembled holes in a doublet show a linear dependence on the template CD along the major axis (see Fig. 9 in Appendix C), a high LCDU in SOC leads to larger variations in this center-to-center distance and consequently larger PE in this direction. Finally, due to the larger variability after lithography, the PE-Y for D3 is already high in SOC (5.4 nm), prior to the DSA

process. We estimate that a PE-Y of ~4.5 nm in SiN for all doublets should be achievable by reducing variability in SOC with better OPC. The average positional variability of the doublets along the horizontal direction (3.2 nm 3σ) does not differ significantly from the value of the singlets (3.0 nm 3σ) as both the confinement within the doublet and the variability of the doublet template in this direction are comparable to the situation of a singlet.

Tables 1 and 2 also report the pattern variability in edge placement error (EPE) that was derived from the 3σ values for LCDU and PE as follows:

$$\mathrm{EPE} = \sqrt{\left(\frac{\mathrm{LCDU}}{2}\right)^2 + \mathrm{PE}^2}. \quad (1)$$

Remarkably, the overall EPE-Y values are significantly reduced after the DSA process and transfer into SiN, from 4.9 and 8.9 nm 3σ in SOC to 4.0 and 6.3 nm 3σ in SiN for singlets and doublets, respectively. This is a result of the large LCDU of the templates in SOC in combination with the rectifying properties of the self-assembly process. This EPE reduction should be put in perspective; for the reported individual features (S1, S2, S3, D1, D2, and D3), a slight increase in EPE is observed instead. It is clear that with a more optimized OPC, and as a result a lower overall LCDU of the SOC templates, the impact of the rectifying properties of the self-assembly process on the EPE will be reduced as well.

Although it is difficult to make a true comparison, the obtained results in terms of pattern variability (in the order of 3 to 4 nm 3σ) are in line with industry expectations,[1] as well as recent results in the field for via patterning found in the literature, either with a similar process[28] or with extreme ultraviolet lithography[29] (both obtained on periodic designs). However, caution should be used when comparing 3σ values. Generally, these values are interpreted assuming a normal distribution to get a rough probability estimate of, e.g., a 6σ event. It should be pointed out that actual data from these processes typically show deviations from a normal distribution at the outer extremities of the curve[30] (exactly the regions that impact the yield). It is likely that different stochastic processes lead to distinct behavior in these tail regions, which is not grasped by simply measuring a standard deviation. Since the displacement of a BCP domain in graphoepitaxy DSA is limited by the confinement boundaries, one may expect a probability distribution curve with a shorter tail compared with most stochastic processes in lithography. More research on this topic is needed and beyond the scope of this work.

To add another perspective, a recent simulation study by Karageorgos et al.[31] has pointed out that via variabilities up to 7 nm 3σ in LCDU and PE have a negligible impact on device performance as the via resistance is a small fraction of the total resistive path of a digital circuit. As long as the via is properly metallized and there is a minimal contact area, the obtained variabilities are of no concern for device performance.

4 Conclusions

The patterning of a via layer from an actual 7-nm node logic layout using [litho-etch-DSA-etch]×2 was demonstrated. The use of feature multiplication in the form of doublets (two-hole features) allows for the significant reduction in the number of masks and thus cost. The pattern quality in terms of defects and variability was investigated thoroughly on full wafer scale. Most of the observed defects (20 per 14,985 holes) are caused by suboptimal mask design and OPC. The self-organizing nature of the assembly process allows a significant decrease in dimensional variability at the cost of a slight increase in positional variability. In the end, the overall edge placement variability is still substantially reduced. The obtained variability of the patterns is comparable to the recent results in the field. In addition, a clear pathway to improved pattern quality exists by adjusting the mask design and optimizing OPC. No major obstacles for insertion of graphoepitaxy DSA for hole multiplication into device manufacturing were seen.

Appendix A: Intrawafer Process Uniformity

As previously mentioned in Sec. 2, the 3σ values for PE were calculated using values from all measured dies to get a larger sample size (315 measurements) per feature. This can be justified as the template dimensions and the stochastic processes under investigation only show a negligible signature across the dies under investigation, as shown in the wafer maps in Fig. 7.

Appendix B: Observed Defects

Figure 8 shows the defect counts per individual feature. It can be seen that the defects occur predominantly on

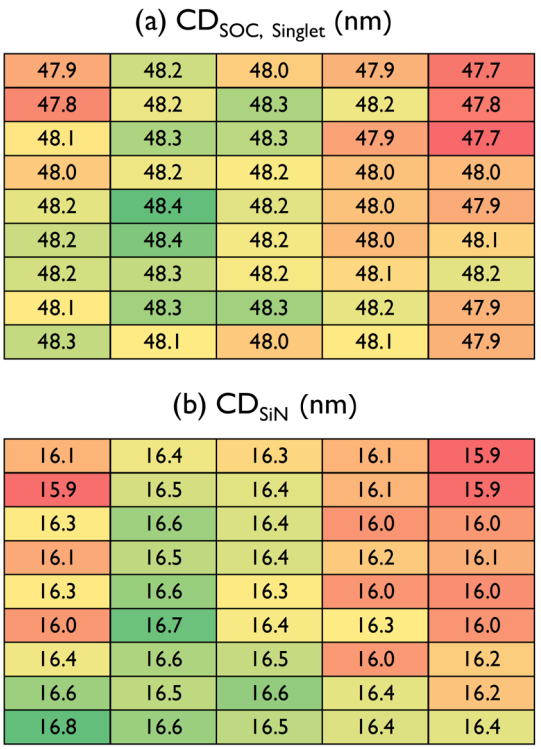

Fig. 7 Wafer maps showing the average CD of (a) singlet templates in SOC and (b) holes in SiN per die.

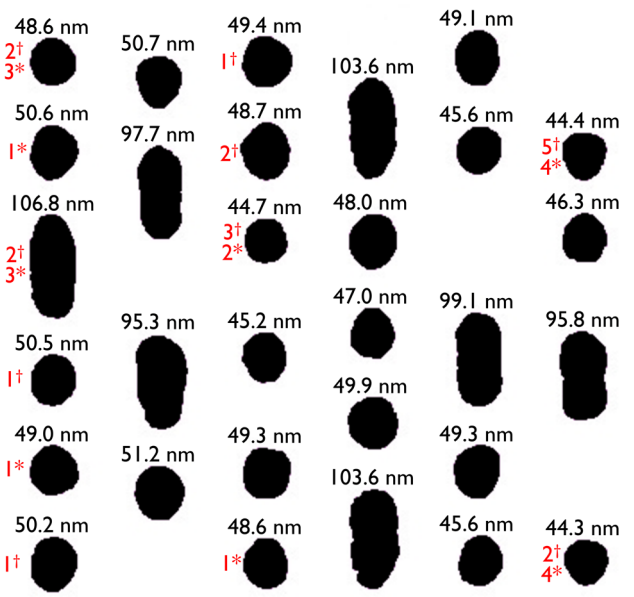

Fig. 8 Defect counts after DSA† and after pattern transfer into SiN* per feature with given SOC dimensions. For doublets, the diameter along the major axis is given; the average diameter is given for singlets. Reported values are averages of all locations on all dies.

the smallest singlet templates and the largest doublet templates.

Appendix C: Center-to-Center Distance of Doublets

Figure 9 shows the linear relationship between center-to-center distance of assembled holes in a doublet and the major axis diameter of the corresponding template. In addition, it can be seen that a lower film thickness (and thus fill level) results in a larger center-to-center distance.

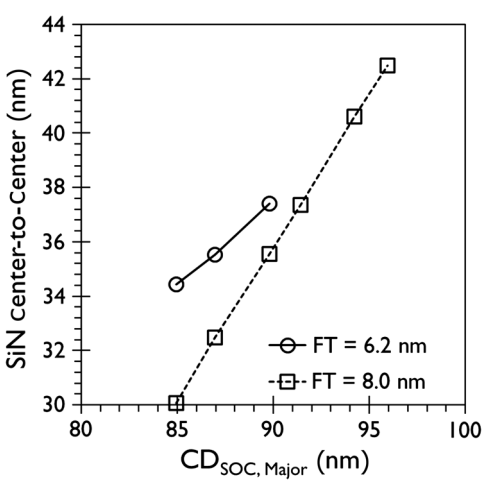

Fig. 9 Center-to-center distance of doublets measured after transfer into SiN as a function of template CD measured along the major axis in SOC and BCP film thickness (FT). To generate this data, two wafers were processed identically except for a different spin speed during the BCP coating. The BCP film thickness refers to the thickness measured with ellipsometry after doing the corresponding BCP coating process on a bare wafer without topography. Reported center-to-center distances are averages of 1000 measurements performed on periodic designs. The wafer with the lower FT showed merging doublets in SiN for the larger templates.

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Biographies for the authors are not available.